

High Performance TFT-LCD Graphics Controller

Introduction

LT7381 is a high-performance TFT-LCD graphics accelerated display controller. Its main function is to assist MCU to display the contents of the TFT screen to the TFT Driver. It provides graphics acceleration, PIP (picture-in-picture), geometry graphics and other functions, in addition to enhance the display efficiency, Also greatly reduces the MCU processing graphics display time spent. LT7381 also supports a very broad display resolution, can be from 320*240(QVGA) to 1024*768(XGA), the display is supported 16/18/24bits RGB interface.



LT7381 supports a variety of MCU interface, including SPI, I2C serial port, or 8-bit, 16-bit parallel interface. In order to achieve multi-layers high-resolution display effect, LT7381 embedded a 32MB Display RAM.

This Display Memory can support 16M color display from 2 gray to 1bit per pixel to up to 24bits per pixel. At the same time to reduce the animation display MCU in the software operation burden. LT7381 built-in geometry drawing engine, supporting the painting point, drawing Line, drawing curve, ellipse, triangle, rectangle, rounded rectangle and other functions. The embedded hardware graphics Acceleration Engine (BTE) provides the command type of graphics operations, such as display rotation, mirror shot, The painting (PIP/Master-Sub Screen) and graphics mixed transparent display and other functions, enhance the display of the product performance, so can greatly reduce the MCU software operating burden. if use the high-speed SPI interface, then it can reduce the MCU I/O port needs, without to upgrade the MCU for TFT display. LT7381 powerful display function is very suitable for the electronic products with TFT-LCD screen, such as home appliances, multi-functional business machines, industrial equipment, industrial control, electronic equipment, medical equipment, human-computer interface, testing equipment and other products.

Internal Block Diagram

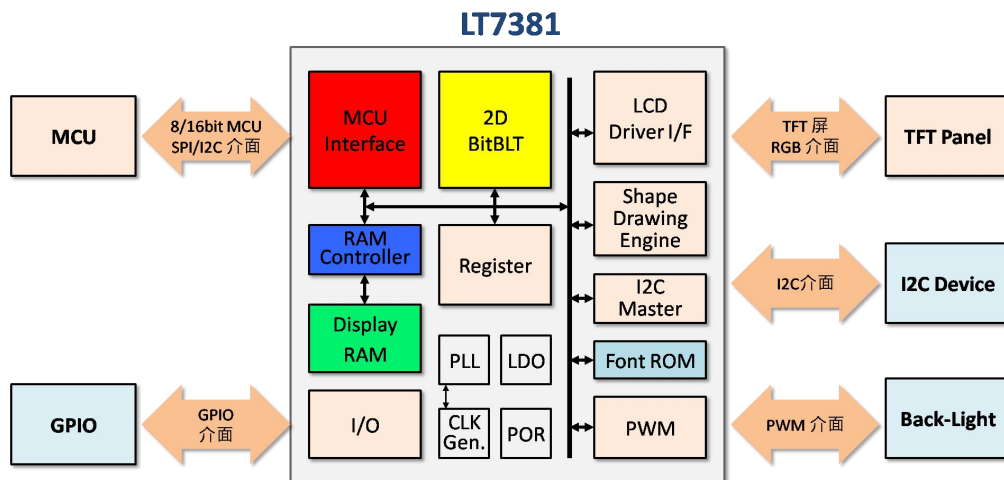


Figure A-1: Internal Block Diagram

System Block Diagram

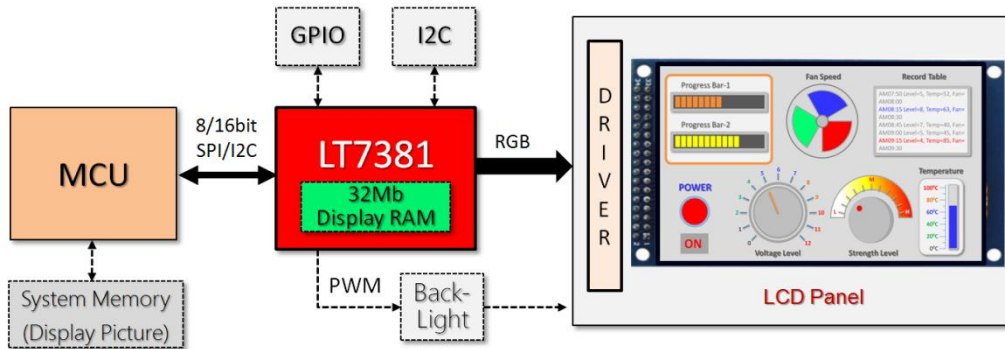


Figure A-2: LT7381 Designed on System Board

Model Name

Table A-1: Model Selection

Model Name	Package	Embedded Display RAM	Resolution (Max.)	Colors
LT7381	LQFP-128	32Mb	1024*768	16.7M

Pin Assignment

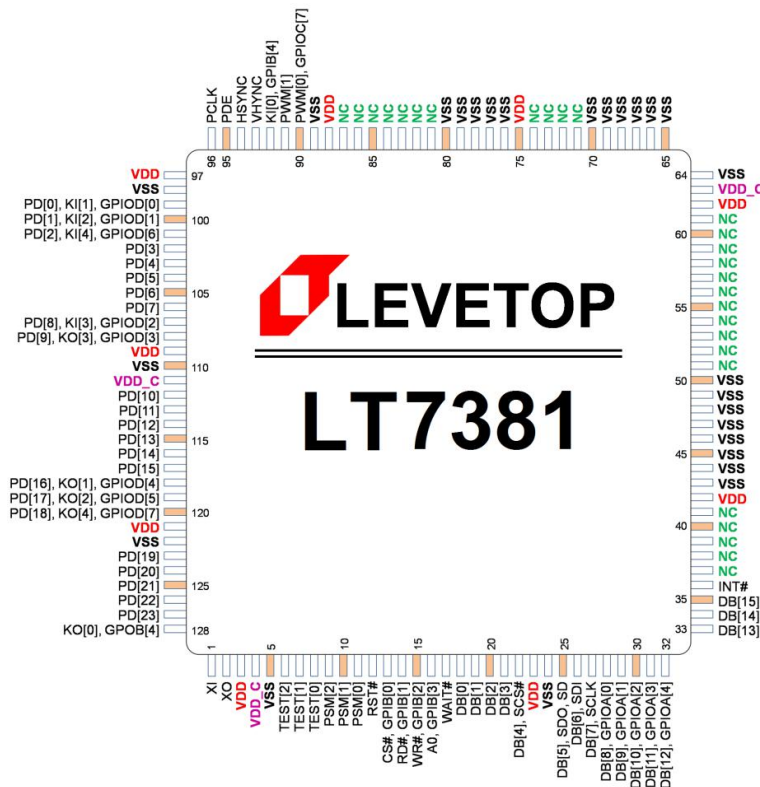


Figure A-3: LT7381 Pin Assignment (LQFP-128Pin)

Features

Host Interface

- Support Three Types 8/16bits Asynchronous Bus Register Interface (or Memory Data)
 - Indirect Intel-80 Bus Interface
 - Indirect Motorola-6800 Bus Interface
- Provides Insert Wait State Mechanism on Parallel Host Cycle
- Support I²C Bus Interface
- Support Various SPI Protocol. Ex. 3 or 4-wire SPI

Display Data Formats

- 1bpp: Monochrome Data (1-bit/Pixel)
- 8bpp: RGB 3:3:2 (1-byte/Pixel)
- 16bpp: RGB 5:6:5 (2-byte/Pixel)
- 24bpp: RGB 8:8:8 (3-byte/Pixel or 4-byte/Pixel)
- Index 2:6 (64 Index Colors/Pixel with Opacity Attribute)
- αRGB 4:4:4 (4096 Colors/Pixel with Opacity Attribute)

Support Panel and Resolution

- Support 16/18/24-bits RGB Interface Type Panel
- Supported Resolution:
 - QVGA : 320*240, 16/18/24-bit LCD Panel
 - WQVGA: 480*272, 16/18/24-bit LCD Panel
 - VGA : 640*480, 16/18/24-bit LCD Panel
 - WVGA : 800*480, 16/18/24-bit LCD Panel
 - SVGA : 800*600, 16/18/24-bit LCD Panel
 - QHD : 960*540, 16/18/24-bit LCD Panel
 - WSVGA: 1024*600, 16/18/24-bit LCD Panel
 - XGA : 1024*768, 16/18/24-bit LCD Panel

Display Functions

- Multiple Display Buffer: Multi buffering allows the main display window to be switched among buffers. Multi buffering allows a simple animation display to be performed by switching the buffers
- Horizontal/Vertical Flip Display: Vertical Flip display functions are available for image data reads. PIP window will be disabled if flip display function enable

- Mirror and Rotation Functions are Available for Image Data Writes
- Provide four User-defined 32*32 Pixels Graphic Cursor
- Virtual Display: Virtual display is available to show an image which is larger than LCD panel size. The image may scroll easily in any direction
- Picture-in-Picture (PIP) Display: Supported two PIP windows area: Enabled PIP windows are always displayed on top of Main window. The PIP1 window is always on top of PIP2 window
- Wake-up Display: Wake-up Display is available to show the display data quickly which data is stored in Display RAM. This feature is used when returning from the Standby mode or Suspend mode
- Initial Display: Embedded a tiny processor with 12 instructions and use to show display data which stored in the serial flash and need not external MPU participate. It will auto execute after power-on, until program execute complete then handover control rights to external MCU
- Color Bar: It could display color bar on panel directly. Default resolution is 640 dots by 480 dots

Bit Block Transfer Engine (BTE)

- 2D BTE Engine
- Copy Image with Raster Operators
- Color Depth Conversion
- Solid Fill & Pattern Fill
- Provide User-defined Patterns with 8*8 Pixels or 16*16 Pixels
- Opacity (Alpha-Blend) Control: It blends two images and then generates a new image
 - Chroma-Keying Function: Mixes images with applying the specified RGB color according to transparency rate
 - Window Alpha-Blending Function: Mixes two images according to transparency rate in the specified region (fade-in and fade-out functions are available)
 - Dot Alpha-Blending Function: Mixes images according to transparency rate when the target is a graphics image in the RGB format

Display RAM (Frame Buffer)

- Embedded 32Mb Display RAM

Shape Drawing Engine

- Provide Smart Drawing Features: Line, Rectangle, Triangle, Polygon, Poly-Line, Circle, Ellipse, Arc, Rounded-Rectangle and Circle-Rectangle

Text Features

- Embedded 8*16, 12*24, 16*32 Character Sets of ISO/IEC 8859-1/2/4/5
- User-defined Characters Support Half Size & Full Size for 8*16, 12*24 and 16*32
- Programmable Text Cursor for Writing with Character
- Character Enlargement Function *1, *2, *3, *4 for Horizontal/Vertical Direction
- Support Character Rotates 90 Degree

PWM Interface

- Embedded Two 16bits Timers
- One 8-bit Pre-Scalars & One 4bits Divider
- Programmable Duty Control of Output Waveform (PWM)
- Auto Reload Mode or One-Shot Pulse Mode
- Dead-Zone Generator

Key-Matrix Interface

- Support up to 5*5 key matrix
- Programmable Scan Period
- Support Long Key & Repeat Key
- Support up to Two Keys Pressed Simultaneously
- Support Keypad-Scan Wakeup function

I2C Interface

- Support Standard Mode (100kbps) and Fast Mode (400kbps)

Power Saving

- Support Three Kind of Power Saving Mode: Standby, Suspend and Sleep Mode
- Support Wakeup Function by Host and External Event

Clock Source

- Embedded Programmable PLL for Core Clock, LCD Panel's Pixel Clock and Frame Buffer Clock

Reset

- Provide Power On Reset Automatically
- Accept External Hardware Reset to Synchronize with System
- Software Command Reset

Power Supply

- VDD: 3.3V +/- 0.3V
- Embedded 1.8V LDO

Package

- LQFP-128Pins

Temperature

- -40°C~85°C

Pin Description

Host Interface Select Signals (3 Pins)

Table A-2: Host I/F Select Signals

Pin #	Pin Name	I/O	Pin Description												
9~11	PSM[2:0]	I	Host Interface Selection <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>PSM[2:0]</th> <th>Host I/F Mode</th> </tr> </thead> <tbody> <tr> <td>0 0 X</td> <td>8bits or 16bits 8080 Parallel Interface Mode</td> </tr> <tr> <td>0 1 X</td> <td>8bits or 16bits 6800 Parallel Interface Mode</td> </tr> <tr> <td>1 0 0</td> <td>3-Wire SPI Mode</td> </tr> <tr> <td>1 0 1</td> <td>4-Wire SPI Mode</td> </tr> <tr> <td>1 1 X</td> <td>I2C Mode</td> </tr> </tbody> </table> <p>If Host interface set as parallel mode, then PSM[0] pin is external interrupt input pin.</p>	PSM[2:0]	Host I/F Mode	0 0 X	8bits or 16bits 8080 Parallel Interface Mode	0 1 X	8bits or 16bits 6800 Parallel Interface Mode	1 0 0	3-Wire SPI Mode	1 0 1	4-Wire SPI Mode	1 1 X	I2C Mode
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Host Parallel I/F Signals (22 Pins)

Table A-3: Host Parallel I/F Signals

Pin #	Pin Name	I/O	Pin Description
35~25, 22~18	DB[15:0]	IO	Host Data Bus These are data bus for data transfer between Host and LT7381. DB[15:8] will become GPIO (GPIOA[7:0]) when parallel Host 8080/6800 16-bits data bus mode doesn't set. DB[7:0] are multiplex pins that share with Serial Host control pins. When serial host mode set then DB[7:0] are defined as the control pins of serial host. Please refer to Host Interface section.
13	CS# GPIB[0]	I	Chip Select Input Low active chip select pin from Host. If host interface set as serial host mode, then this pin can be set as GPIB[0]. This pin with an internal pull-high resistor.
14	RD# EN GPIB[1]	I	Read / Enable Input RD#: When host interface is 8080 mode then this is a Read input signal, active low. EN: When interface is 6800 mode then this is a Enable input signal, active high. If host interface set as serial host mode then this pin can be set as GPIB[1]. This pin with an internal pull-high resistor.

Table A-3: Host MCU Parallel I/F Signals (Continued)

Pin #	Pin Name	I/O	Pin Description
15	WR# RW# GPIB[2]	I	<p>Write / Read-Write Input</p> <p>WR#: When host interface is 8080 mode then this is a Write input signal, active low.</p> <p>RW#: When interface is 6800 mode then this is a Read-Write input signal. It active high in 'Host's read cycle, and active low in Host's write cycle.</p> <p>If host interface set as serial host mode then this pin will be set as GPIB[2]. This pin with an internal pull-high resistor.</p>
16	A0 GPIB[3]	I	<p>Command / Data Select Input</p> <p>The pin is used to select Command or Data cycle.</p> <p>A0 = 0, Status Read or Command Write cycle is selected.</p> <p>A0 = 1, Data Read or Data Write cycle is selected.</p> <p>If host interface set as serial host mode then this pin will be set as GPIB[3]. This pin with an internal pull-high resistor.</p>
36	INT#	O	<p>Interrupt Output Signal</p> <p>The interrupt output for host to indicate the status.</p>
17	WAIT#	O	<p>Wait Output Signal</p> <p>When high, it indicates that the LT7381 is ready to transfer data. When low, then microprocessor is in wait state.</p>

MCU Serial I/F Signals (8 Pins)
Table A-4: Host Serial I/F Signals

Pin #	Pin Name	I/O	Pin Description
27	SCLK (DB[7])	I	<p>SPI or I2C Clock</p> <p>SCLK: Clock of 3-wire, 4-wire Serial or I2C interface.</p> <p>This is a multiplex pin that share with Parallel Host Data Bus DB[7].</p>
26	SDI I2C_SDA (DB[6])	I	<p>I2C Data / 4-wire SPI Data Input</p> <p>SDI: Data input pin of 4-wire SPI I/F. Connect to MCU's MOSI.</p> <p>I2C_SDA: Bi-direction data pin of I2C I/F.</p> <p>This pin is not used In 3-Wire serial I/F. Please connect it to GND. This is a multiplex pin that share with Parallel Host Data Bus DB[6].</p>
25	SD SDO I2CA[5] (DB[5])	IO	<p>3-wire SPI Data / 4-wire SPI Data Output / I2C Slave Address Select</p> <p>SD: Bi-direction data pin of 3-wire SPI I/F.</p> <p>SDO: Data output pin of 4-wire SPI I/F. Connect to MCU's MISO.</p> <p>I2CA[5]: I2C device address bit[5] of I2C I/F.</p> <p>This is a multiplex pin that share with Parallel Host Data Bus DB[5].</p>

Table A-4: Host Serial I/F Signals (Continued)

Pin #	Pin Name	I/O	Pin Description
22	SCS# I2CA[4] (DB[4])	I	SPI Chip Select / I2C Slave Address Select SCS#: Chip select pin for 3-wire or 4-wire serial I/F. I2CA[4]: I2C device address bit[4]. This is a multiplex pin that share with Parallel Host Data Bus DB[4].
21~18	I2CA[3:0] (DB[3:0])	I	I2C Slave Address Select I2CA[3:0]: I2C device address bit [3:0]. These pins are not used In 3-Wire or 4-Wire I/F. Please connect them to GND. These are multiplex pins that share with Parallel Host Data Bus DB[3:0].

PWM Output Signals (2 Pins)

Table A-5: PWM Output Signals

Pin #	Pin Name	I/O	Pin Description
90	PWM[0] INITDIS GPIOC[7] CCLK	IO	PWM Output 0 / Initial Display Enable PWM[0]: PWM's output signal. The output mode is decided by configuration register. This pin can be used as the control signal of TFT panel's back light. INITDIS: Pull-high this pin will enable Initial Display function. This pin has internal pull-down in reset period to disable Initial Display function by default. i.e. after reset complete, internal pull-down resistor will be disabled. If PWM function disabled then it can be programmed as GPIO C[7], and default is GPIOC[7] input function, or output Core Clock - CCLK.
91	PWM[1]	IO	PWM Output 1 PWM's output signal. The output mode and output function is decided by configuration register. This pin also can be used as the control signal of TFT panel's back light. When TEST[0] set high, then PWM[1] pin is external panel scan clock input

LCD Driver Signals (28 Pins)

Table A-6: LCD Driver Signals

Pin #	Pin Name	I/O	Pin Description																																																																																																																																	
127~123, 120~112, 108~99	PD[23:0]	IO	<p>LCD Panel Data Bus</p> <p>TFT LCD data bus output for source driver. LT76x supports 64K/256K/16.7M color depth by register setting; user can connect corresponding RGB bus for different setting.</p> <table border="1" style="margin: 10px auto;"> <thead> <tr> <th rowspan="2">Pin Name</th> <th colspan="4">TFT-LCD Interface</th> </tr> <tr> <th>11b (GPIO)</th> <th>10b (16bits)</th> <th>01b (18bits)</th> <th>00b (24bits)</th> </tr> </thead> <tbody> <tr> <td>PD[0]</td> <td colspan="3">GPIOD[0] / KI[1]</td> <td>B0</td> </tr> <tr> <td>PD[1]</td> <td colspan="3">GPIOD[1] / KI[2]</td> <td>B1</td> </tr> <tr> <td>PD[2]</td> <td colspan="2">GPIOD[6] / KI[4]</td> <td>B0</td> <td>B2</td> </tr> <tr> <td>PD[3]</td> <td>GPIOE[0]</td> <td>B0</td> <td>B1</td> <td>B3</td> </tr> <tr> <td>PD[4]</td> <td>GPIOE[1]</td> <td>B1</td> <td>B2</td> <td>B4</td> </tr> <tr> <td>PD[5]</td> <td>GPIOE[2]</td> <td>B2</td> <td>B3</td> <td>B5</td> </tr> <tr> <td>PD[6]</td> <td>GPIOE[3]</td> <td>B3</td> <td>B4</td> <td>B6</td> </tr> <tr> <td>PD[7]</td> <td>GPIOE[4]</td> <td>B4</td> <td>B5</td> <td>B7</td> </tr> <tr> <td>PD[8]</td> <td colspan="3">GPIOD[2] / KI[3]</td> <td>G0</td> </tr> <tr> <td>PD[9]</td> <td colspan="3">GPIOD[3] / KO[3]</td> <td>G1</td> </tr> <tr> <td>PD[10]</td> <td>GPIOE[5]</td> <td>G0</td> <td>G0</td> <td>G2</td> </tr> <tr> <td>PD[11]</td> <td>GPIOE[6]</td> <td>G1</td> <td>G1</td> <td>G3</td> </tr> <tr> <td>PD[12]</td> <td>GPIOE[7]</td> <td>G2</td> <td>G2</td> <td>G4</td> </tr> <tr> <td>PD[13]</td> <td>GPIOF[0]</td> <td>G3</td> <td>G3</td> <td>G5</td> </tr> <tr> <td>PD[14]</td> <td>GPIOF[1]</td> <td>G4</td> <td>G4</td> <td>G6</td> </tr> <tr> <td>PD[15]</td> <td>GPIOF[2]</td> <td>G5</td> <td>G5</td> <td>G7</td> </tr> <tr> <td>PD[16]</td> <td colspan="3">GPIOD[4] / KO[1]</td> <td>R0</td> </tr> <tr> <td>PD[17]</td> <td colspan="3">GPIOD[5] / KOI[2]</td> <td>R1</td> </tr> <tr> <td>PD[18]</td> <td colspan="2">GPIOD[7] / KO[4]</td> <td>R0</td> <td>R2</td> </tr> <tr> <td>PD[19]</td> <td>GPIOF[3]</td> <td>R0</td> <td>R1</td> <td>R3</td> </tr> <tr> <td>PD[20]</td> <td>GPIOF[4]</td> <td>R1</td> <td>R2</td> <td>R4</td> </tr> <tr> <td>PD[21]</td> <td>GPIOF[5]</td> <td>R2</td> <td>R3</td> <td>R5</td> </tr> <tr> <td>PD[22]</td> <td>GPIOF[6]</td> <td>R3</td> <td>R4</td> <td>R6</td> </tr> <tr> <td>PD[23]</td> <td>GPIOF[7]</td> <td>R4</td> <td>R5</td> <td>R7</td> </tr> </tbody> </table>	Pin Name	TFT-LCD Interface				11b (GPIO)	10b (16bits)	01b (18bits)	00b (24bits)	PD[0]	GPIOD[0] / KI[1]			B0	PD[1]	GPIOD[1] / KI[2]			B1	PD[2]	GPIOD[6] / KI[4]		B0	B2	PD[3]	GPIOE[0]	B0	B1	B3	PD[4]	GPIOE[1]	B1	B2	B4	PD[5]	GPIOE[2]	B2	B3	B5	PD[6]	GPIOE[3]	B3	B4	B6	PD[7]	GPIOE[4]	B4	B5	B7	PD[8]	GPIOD[2] / KI[3]			G0	PD[9]	GPIOD[3] / KO[3]			G1	PD[10]	GPIOE[5]	G0	G0	G2	PD[11]	GPIOE[6]	G1	G1	G3	PD[12]	GPIOE[7]	G2	G2	G4	PD[13]	GPIOF[0]	G3	G3	G5	PD[14]	GPIOF[1]	G4	G4	G6	PD[15]	GPIOF[2]	G5	G5	G7	PD[16]	GPIOD[4] / KO[1]			R0	PD[17]	GPIOD[5] / KOI[2]			R1	PD[18]	GPIOD[7] / KO[4]		R0	R2	PD[19]	GPIOF[3]	R0	R1	R3	PD[20]	GPIOF[4]	R1	R2	R4	PD[21]	GPIOF[5]	R2	R3	R5	PD[22]	GPIOF[6]	R3	R4	R6	PD[23]	GPIOF[7]	R4	R5	R7
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<p>These are multiplex pins that share with GPIO and Key-Matrix pins. The Default setting of LCD I/F is 18bpp function mode, so PD[17:16 / 8:9 / 1:0] are defined as GPIO pins.</p>																																																																																																																																				

Table A-6: LCD Driver Signals (Continued)

Pin #	Pin Name	I/O	Pin Description
96	PCLK	O	Panel Scan Clock Generic TFT interface signal for panel scan clock. It derives from internal PLL.
93	VSYNC	O	VSYNC Pulse Generic TFT interface signal for vertical synchronous pulse.
94	HSYNC	O	HSYNC Pulse Generic TFT interface signal for horizontal synchronous pulse.
95	PDE	O	Data Enable Generic TFT interface signal for data valid or data enable.

GPIO Signals (28 Pins)
Table A-7: General Purpose I/O Signals

Pin #	Pin Name	I/O	Pin Description
35~28	GPIOA[7:0]	IO	GPIO A Group These are general purpose I/O. These are multiplex pins that share with DB[15:8]. They are available when 8bits parallel host mode and serial Host mode.
92, 128, 16~13	GPIB[4], GPOB[4], GPIB[3:0]	IO	GPIO B Group These are general purpose I/O. GPIB[3:0] are read only and available in serial host mode. GPIB[4] is same pin with KI[0]. GPOB[4] is same pin with KO[0]. GPIB[3:0] are multiplex pins that share with {A0, WR#, RD#, CS#}.
90, 38, 37, 41~39	GPIOC[7], GPIOC[4:0]	IO	GPIO C Group These are general purpose I/O. GPIOC are available when PWM and SPI Master functions disabled. GPIOC[7] is same pin with PWM[0]. GPIOC[4:0] are multiplex pins that share with {SFCS1#, SFCS0#, SFDI, SFDO, SFCLK}
120, 101 119, 118 108, 107 100, 99	GPIOD[7:0]	IO	GPIO D Group These are general purpose I/O. GPIOD[7:0] are multiplex pins that share with PD[18, 2, 17, 16, 9, 8, 1, 0]. GPIOD[5,4,3,2,1,0] are available when LCD Panel interface is set 16bits or 18bits. GPIOD[7,6] are available when LCD Panel interface is set 16bits.

Key-Matrix Signals (10 Pins)
Table A-8: Key-Matrix Signals

Pin #	Pin Name	I/O	Pin Description
101, 107, 100, 99, 92	KI[4:0]	I	Key-Matrix Data Pins Keypad data inputs with internal pull-up resister. KI[4:1] are multiplex pins that share with PD[8] and PD[2:0]. The Key-matrix function will be disable when LCD I/F are set as 24bits. XKIN[0] also provide the I2CMCK function of I2C Master.
120,108, 119,118, 128	KO[4:0]	O	Key-Matrix Strobe Pins Keypad strobe data outputs with Open-Drain. KO[4:1] are multiplex pins that share with PD[9] and PD[18:16]. KO[0] also provide the I2CMDA function of I2C Master.

Power and Clock Signals (40 Pins)
Table A-9: Power and Clock Signals

Pin #	Pin Name	I/O	Pin Description
1	XI	I	Crystal / External Clock Input This input pin is used for internal crystal circuit or external clock that generate clock source for PLL. It should be connected to external crystal or clock and suggested frequency is 10.0MHz.
2	XO	O	Crystal Output This is an output pin for internal crystal circuit. It should be connected to external crystal circuit.
4, 63, 111	VDD_C	PWR	Internal LDO Output These pins must connect 1uF and 0.1uF capacitor to ground.
3, 23, 42, 62, 75, 88, 97, 109, 121	VDD	PWR	3.3V Power Pins
5, 24, 43~50, 64~70, 76~80, 89 98, 110, 122	VSS	PWR	Ground(GND) Pins

Reset and Test Signals (4 Pins)**Table A-10: Reset and Test Signals**

Pin #	Pin Name	I/O	Pin Description
12	RST#	I/O	Reset Signal Input This is a active low Reset pin for LT7381. To avoid noise interfere and cause fake reset behavior, this pin is active at least 256 OSC clocks.
6~8	TEST[2:0]	I	Test Input These pins are used for testing and normally connect to GND. If TEST[0] keep high, the internal PLL will be disable and the system clock is supply by external. If TEST[2:1] keep 01b, then the SPI Master signals will keep floating. This feature allow external device to program Serial Flash directly. (i.e. ISP, In-System-Programming)

Package Information

LT7381 (LQFP-128pin)

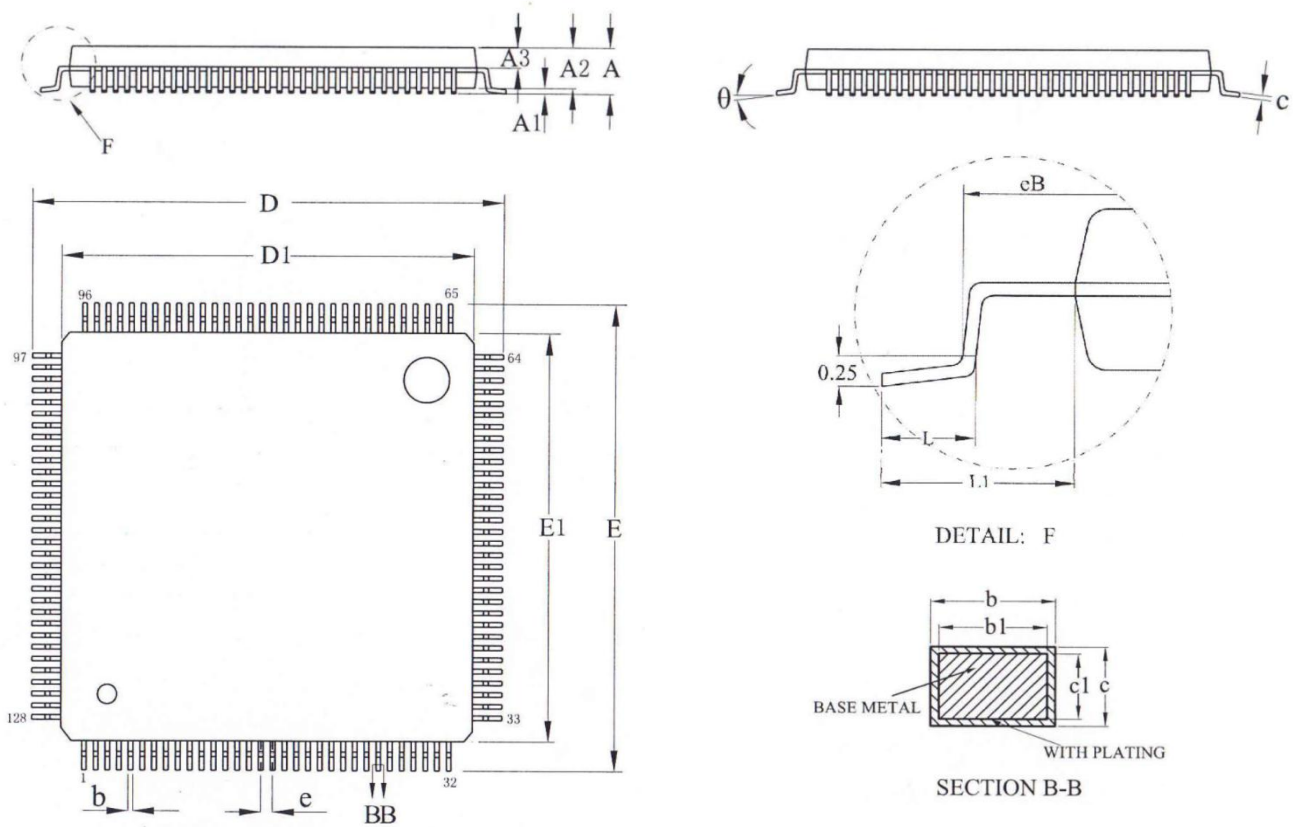


Figure B-1: 128Pin LQFP Outline

Table B-1: 128Pin LQFP Dimension

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	-	-	1.60	D1	13.9	14.0	14.1
A1	0.05	-	0.15	E	15.8	16.0	16.2
A2	1.35	1.40	1.45	E1	13.9	14.0	14.1
A3	0.59	0.64	0.69	eB	15.05	-	15.35
b	0.14	-	0.22	e	0.40BSC		
b1	0.13	0.16	0.19	L	0.45	-	0.75
c	0.13	-	0.17	L1	1.00REF		
c1	0.12	0.13	0.14	θ	0		7
D	15.8	16.00	16.2				